UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte WINTHROP L. SAVILLE and KEVIN ROSS

Appeal No. 2005-0869
Application No. 09/391,647

ON BRIEF

Before: JERRY SMITH, BLANKENSHIP and NAPPI, **Administrative Patent Judges**.

NAPPI, **Administrative Patent Judge**.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 of the final rejection of claims 14 through 26. For the reasons stated *infra* we affirm-in-part the examiner's rejection of these claims.

Invention

The invention relates to the formation of instructions in a processing system. The instructions include an opcode portion and a parameter portion. See page 1 of appellants' specification. The invention reduces the memory space needed by compressing parameters without increasing the number of opcodes. The method provides a compressible parameter portion where the parameter portion includes an expansion indicator which represents whether or not the parameter portion is compressed. See page 3 of appellants' specification.

Claim 14 is representative of the invention and is reproduced below:

> 14. A method of forming instructions for execution in a processing system, said method comprising:
>
> providing an opcode portion determining at least one instruction to be performed by the processing system; and
>
> providing a first parameter byte including a first set of data value bits, and a first expansion bit indicative of whether the processing system expands the first set of data value bits or reads any additional parameter bytes including additional sets of data value bits.

References

The reference relied upon by the examiner is:

Matsumoto et al. (Matsumoto)	4,454,578	Jun. 12, 1984

Rejection at Issue

Claims 14 through 26 stand rejected under 35 U.S.C. § 102 as being anticipated by Matsumoto.

Opinion

We have carefully considered the subject matter on appeal, the rejection advanced by the examiner and the evidence of anticipation relied upon by the examiner as support for the rejection. We have, likewise, reviewed and taken into consideration, in reaching our decision, the appellants' arguments set forth in the brief along with the examiner's rationale in support of the rejection and arguments in rebuttal set forth in the examiner's answer.

With full consideration being given to the subject matter on appeal, the examiner's rejection and the arguments of appellants and the examiner, and for the reasons stated *infra* we sustain the examiner's rejections of claims 20, 21, and 23 through 26 under 35 U.S.C. § 102. However, we will not sustain the examiner's rejection of claims 14 through 19 and 22 under 35 U.S.C. § 102.

Grouping of the claims.

At the outset, we note that appellant states, on page 7of the brief, that:

> The claims should be considered in two (2) separate groups:
> Group I includes representative claim 14 and claims 15-19 depending from claim 14, all of which specify a method of forming instructions for execution in a processing system.
>
> Group II is dependent claim 22, which specifies a method of forming instructions for execution in a processing system.

37 C.F.R. § 1.192(c) (7) (July 1, 2003) as amended at 62 Fed. Reg. 53196 (October 10, 1997), which was controlling at the time of appellant filing the brief, states:

> For each ground of rejection which appellant contests and which applies to a group of two or more claims, the Board shall select a single claim from the group and shall decide the appeal as to the ground of rejection on the basis of that claim alone unless a statement is included that the claims of the group do not stand or fall together and in the argument under paragraph (c) (8) of this section appellant explains why the claims of the group are believed to be separately patentable. Merely pointing out differences in what the claims cover is not an argument as to why the claims are separately patentable.

Appellants have not identified how claims 20, 21 and 23 through 26 are to be grouped. Accordingly, we will consider the claims in three groups, Group 1, consisting of claims 14 through 19, with claim 14 as the representative claim, Group 2 consisting of claim 22, and Group 3 consisting of claims 20, 21 and 23 through 26.

Rejection of claims in Group 1 (Claims 14 through 19).

We first consider the rejection of claims 14 through 19 under 35 U.S.C. § 102 as being anticipated by Matsumoto. Appellants argue, on page 9 of the brief:

> Matsumoto fails to teach or suggest compression of the LITERAL VALUE fields of the specifiers whereby the LITERAL VALUE fields would have to be expanded during a decoding of the operand specifiers. Thus, Matsumoto falls to disclose, teach or suggest a need for an expansion bit in the operand specifier wherein the expansion bit indicates whether the data bits of the LITERAL VALUE field should be expanded by decoder 505.
>
> Moreover, Matsumoto teaches the short literal mode specifier and the long literal mode specifier are two separate and distinct operand specifiers. Specifically, Matsumoto teaches the long literal mode specifier is to be used whenever a length of the literal data needs to be greater than the 56 bit maximum of the short literal mode specifier. See, Matsumoto at column 2, line 55 to column 3, line 2. Thus, Matsumoto can not be interpreted as proposed by Examiner Ellis that the 000 field of the long literal mode specifier indicates an expansion of the short literal mode specifier, because a substitution of the long literal mode specifier for the

> short literal mode specifier whenever the address is greater then 56 bits negates any purpose for expanding the short literal mode specifier.

Appellants thus, conclude, on page 10 of the brief:

> Matsumoto clearly fails to disclose, teach or suggest "providing a first parameter byte including ... a first expansion bit indicative of whether the processing system expands the first set of data value bits or reads any additional parameter bytes including additional sets of data value bits" as recited in independent claim 14.

In the statement of the rejection, on page 4 of the answer, the examiner equates the three bit "LENGTH" field of Matsumoto to the expansion bit and reasons that when the three bit "LENGTH" bit is "000," the system expands the "LENGTH" field to 8 bits. In response to the appellants' arguments, the examiner states on page 10 of the answer, "appellant's claims do not claim compression of any fields, must [sic, much] less compression of a 'LITERAL VALUE' field." Further, on page 11 of the answer, the examiner responds stating:

> Appellant's claims merely recite "a first set of data value bits" which is a significantly broader phrase then "LITERAL VALUE" field, and as well, merely recite "expand[ing]" the "first set of data value bits", where the word "expand" is significantly broader than the word "compression." As was clearly detailed in the rejection of appellant's claims above, Matsumoto et al. clearly taught " a set of data value bits" and as well clearly taught "expanding" those data value bits exactly as the word "expand" is defined in the English language.

We disagree with the examiner's rationale and do not find that the situation where the three bit "LENGTH" field is "000" meets the claimed expansion limitation. Claim 14 includes the limitation "providing a first parameter byte including a first set of data value bits, and a first expansion bit indicative of whether the processing system expands the first set of data value bits." We

concur with the examiner's interpretation, on page 4 of the answer, of the claim term "expand" as "1: to open up: unfold, 2: to increase the extent, number, or scope of or enlarge." Thus, we find that the scope of the claim includes that an expansion bit is indicative of whether the processing system is to increase or enlarge the data value bits.

Matsumoto teaches a data processing unit which executes variable length instructions. See column 1, lines 63-65. One example, relied upon by the examiner, of the data structures used in the device are shown in figures 1A through 1D. Two of these data structures are the short literal (Fig 1A) and the long literal (Fig 1B). The first bit identifies the type of data, the first bit being a 1 for literal data. See column 2, line 60. We find that there are three differences between the two data structures 1) the long literal has "000" fourth through sixth bit position, where as the short literal has the variable "LENGTH", 2) the long literal has the variable "LENGTH" in the seventh through twelfth bit positions, where as the short literal has "LITERAL VALUE" in these bit positions" 3) the long literal is used to produce data having a longer length then the in the short literal. See figures 1A, 1B, and column 2 line 67 through column 3, line 2. We find, as the examiner asserts, that when the "000" is in the in the fourth through the sixth bit position a long literal mode is indicated, and the length field is 8 bits vice 3 for the short literal.

We do not, however find that the "000" indication identifying that the length field is 8 bits meets the claimed expansion limitation. As discussed, *supra* we

consider the scope of the limitation is that the expansion bit is indicative of whether the processing system is to increase or enlarge the data value bits. The "000" is not indicating to the processing system that the bits in the byte are to be expanded, increased or enlarged, rather the "000" is a indicator that the size field is in the succeeding 8 bits, i.e. the seventh through twelfth bit positions. Thus, we find that Matsumoto does not teach all of the limitations of independent claim 14, nor the limitations of dependent claims 15 through 19. Accordingly, we will not sustain the examiner's rejection of claims 14 through 19 under 35 U.S.C. § 102.

Rejection of claim in Group 2 (Claim 22).

Appellants argue on page 11 of the brief that Matsumoto does not teach or suggest the limitation "wherein the parameter portions further includes a second indicator representative of whether to expand the plurality of data value bits" as claimed in dependent claim 22.

We concur. Claim 22 is multiply dependent upon claims 20 or 21. Both independent claims 20 and 21 are directed to forming instructions for execution on a processing system and include a limitation directed to an opcode portion and a parameter portion containing a plurality of data value bits. Claim 22 adds the limitation, that "the parameter portions further include a second indicator representative of whether to expand the plurality of data value bits." Applying analysis similar to that discussed *supra* with respect to claim 14, we consider the scope of this limitation to require a second indicator that is representative of

whether the data value bits are to be increased or enlarged. As discussed *supra* we do not find that Matsumoto teaches this limitation. Accordingly, we will not sustain the examiner's rejection of claim 22 under 35 U.S.C. § 102.

Rejection of claim in Group 3 (Claims 20, 21 and 23 through 26).

The examiner's rationale in support of the rejection of the claims in this group is set forth on pages 7 through 10 of the brief. We find that the examiner's statements set forth a ***prima face*** case of anticipation. Appellants in their briefs have presented no arguments directed to the claims in this group. Further, the arguments the appellants have made with respect to the other rejected claims, are not applicable to the claims of this group as the limitations argued are not present in these claims, i.e. claims 20, 21 and 23 through 26 do not contain limitations directed to expanding the plurality of data bits. Accordingly, we sustain the examiner's rejection of claims 20, 21 and 23 through 26 under 35 U.S.C. § 102.

Only those arguments actually made by appellant have been considered in this decision. Arguments which appellant could have made but chose not to make in the brief or by filing a reply brief have not been considered and are deemed waived by appellant (see 37 CFR § 41.37(c)(vii)). Support for this rule has been demonstrated by our reviewing court in ***In re Berger*** 279 F.3d 975, 984, 61 USPQ2d 1523, 1528-1529 (Fed. Cir. 2002) wherein the Federal Circuit Court stated that because the appellant did not contest the merits of the

rejections in his brief to the Federal Circuit Court, the issue is waived. ***See also In re Watts*** 354 F.3d 1362, 1368, 69 USPQ2d 1453, 1458 (Fed. Cir. 2004).

In summary, we sustain the examiner's rejections of claims 20, 21, and 23 through 26 under 35 U.S.C. § 102. However, we will not sustain the examiner's rejection of claims 14 through 19 and 22 under 35 U.S.C. § 102. The decision of the examiner is affirmed-in-part.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a)(1)(iv).

AFFIRMED-IN-PART

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